REMARKS

Applicants submit herewith a petition to the Commissioner of Patents to extend the time for response to the Office Action dated January 24, 2003, for one month from April 24, 2003, to May 24, 2003. Note that May 24, 2003 fell on Saturday of a three-day holiday weekend (Monday, May 26,2003 was Memorial Day); hence Applicants are filing this response on Tuesday, May 27, 2003.

These remarks are responsive to the Office Action dated 24 January 2003. Claims 1–11 are pending in the present Application. Claims 1–11 are rejected, and claims 4, 6, and 10 have been objected to for specific informalities. The specification was objected to for including blank serial number lines. The specification and claims 4, 6 and 10 have been amended to address these objections. Additionally, claim 10 has been amended to recite that the first set of logic functions are included in a standard cell. Claims 1–11 remain pending. For the reasons set forth more fully below, Applicant respectfully submits that the remaining claims are allowable. Consequently, reconsideration, allowance and passage to issue are respectfully requested.

The present invention provides a system for allowing "field selection" of functions that are connected to internal bus(es) and to external I/O of an application specific integrated circuit (ASIC). The ASIC includes a standard cell, the standard cell having a plurality of logic functions. The ASIC further includes at least one FPGA interconnect coupled to at least a portion of the logic functions. The FPGA interconnect can be configured to select a particular logic function of the plurality of logic functions. The functional block connections made with internal buses can be significantly wider and faster than buses

brought on chip via external chip I/Os. Further, the ASIC reduces cost because selective bus connections can be made internal to the chip, thus eliminating the need for additional external pins. Finally, the ASIC reduces the cost of the packaged component by allowing the chip to be packaged in a lower pin count package. The ASIC includes standard (non-field-configurable) cells with the FPGA interconnect selectively accessing them (thus the FPGA is a FPGA that is used as an interconnect and not an interconnect used in a FPGA).

35 USC §102 Rejections

Claims 1–10

The Rejection states:

> **Claims 1–10 are rejected under 35 U.S.C. § 102(b) as being anticipated by Agrawal et al. (US 5,26,881).**
>
> **Regarding claims 1–7, Agrawal discloses, in figures 1 and 61-64, an ASIC (programmable gate array shown in fig. 1) comprising:**
>
> **a standard cell (CLBs R1C1-R8C8); a plurality of input output pins (pins connected to IOB 1-110); and at least one FPGA interconnect (PIPs and/or connection to MUX in IOB shown in figures 61-64; see col. 41, lines 21+) coupled to the plurality of I/O pins and the plurality of logic functions, wherein the at least one FPGA interconnect can be configured to select one of the plurality of logic functions (see fig. 16A) utilizing field programming techniques (see PIP in fig. 17); and wherein the one logic function is coupled to an internal bus (see 15 in fig. 16A) via the at least one configured FPGA interconnect.**
>
> **Regarding claims 8 and 9, utilizing at least one FPGA interconnect to correct wiring error which is a reversed bit order wiring error, when the ASIC is utilized on a printed circuit board, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham (2 USPQ2d 1647 (1987).**
>
> **Regarding claims 10 and 11, Agrawal discloses, in figures 1 and 61-64, an ASIC (programmable gate array shown in fig. 1) comprising:**
>
> **a plurality of I/O pins (pins connected to IOB 1-28);**
>
> **a plurality of first logic functions (CLBs R1C1-R1C8 or R2C1-R2C8);**
>
> **a first FPGA interconnect (PIPs and/or connection to MUX in IOB shown in figures 61; see col. 41, lines 21+) coupled between the plurality of I/O pins and the plurality of first logic function, wherein the first FPGA**

interconnect can be configured to select at least one of the plurality of first logic functions (see fig. 16A);

a bus (HBUS1) coupledto the plurality of first logic functions;

a second FPGA interconnect (segment box or switch matrix or PIPs in HBUS1 or HBUS2) coupled between the bus and the plurality of first logic functions, wherein the second FPGA interconnect is configured to connect to one of the plurality of first logic functions to the bus; and

a plurality of second logic functions (CLBs R3C1-R3C8) coupled to the bus.

Applicant respectfully disagrees with the Rejection particularly the characterization of the Agrawal reference. The present invention provides a system for allowing "field selection" of functions that are connected to internal bus(es) and to external I/O of an application specific integrated circuit (ASIC). The ASIC includes a standard cell, the standard cell having a plurality of logic functions. The ASIC further includes at least one FPGA interconnect coupled to at least a portion of the logic functions. The FPGA interconnect can be configured to select a particular logic function of the plurality of logic functions. The functional block connections made with internal buses can be significantly wider and faster than buses brought on chip via external chip I/Os. Further, the ASIC reduces cost because selective bus connections can be made internal to the chip, thus eliminating the need for additional external pins. Finally, the ASIC reduces the cost of the packaged component by allowing the chip to be packaged in a lower pin count package. The ASIC includes standard (non-field-configurable) cells with the FPGA interconnect selectively accessing them (thus the FPGA is a FPGA that is used as an interconnect and not an interconnect used in a FPGA.

The Examiner asserts that Agrawal anticipates the present invention. Applicant respectfully disagrees.

Independent claims 1, 4, 6, 8 and 10 (as claim 10 was amended) each recite that a standard cell is used, and that a FPGA interconnect is used in cooperation with the standard cell. Agrawal does not teach the standard cell as that term is understood. Particularly, the CLB, being configurable, is not a standard cell. The standard cell of the present invention is a non-field-programmable cell. This is understood since, if it were field programmable, the preferred embodiment would not be applicable as the desired function could be selected. Thus, the rejection is not satisfied for this reason alone.

However, the claims also recite an FPGA interconnect that the rejection asserts is satisfied by an interconnect structure in the Agrawal PGA. The rejection mischaracterizes this limitation, as it is an FPGA structure that is used as an interconnect. This distinction is not just semantic, but reflects the distinctions between the claimed invention of a hybrid structure of non-field-programmable standard cells used with an FPGA to interconnect desired functions from the standard cell.

Consequently, since Agrawal does not disclose a standard cell, or the FPGA interconnect, as recited in the present invention, Applicant asserts that the recited invention of independent claims 1, 4, 6, 8 and 10 is different from the Agrawal reference. Therefore, claims 1, 4, 6, 8 and 10 are allowable over the Agrawal reference.

Claims 2, 3, 5, 7, 9 and 11

Since claims 2, 3, 5, 7, 9 and 11 are dependent on claims 1, 4, 6, 8 and 10, the above-articulated arguments related to claims 1, 4, 6, 8 and 10 apply with equal force to claims 2, 3, 5, 7, 9 and 11. Accordingly, claims 2, 3, 5, 7, 9 and 11 are allowable over Agrawal.

Accordingly, Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

Joseph A. Sawyer, Jr.
Sawyer Law Group LLP
Attorney for Applicant
Reg. No. 30,801
(650) 493-4540